

1 WHAT IS CLAIMED IS

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1. A semiconductor device, comprising:
 a semiconductor chip having a top principal
 surface, said semiconductor chip carrying a plurality
 of bump electrodes on said top principal surface;

10 a resin layer covering said top principal
 surface of said semiconductor chip so as to seal said
 semiconductor chip,

 said semiconductor chip and said resin layer
 thereby forming a composite semiconductor structure
15 defined by a side wall having a plurality of corners,
 and

 a chamfer surface formed in said side wall
 of said composite semiconductor structure as a part of
 said side wall such that said chamfer surface extends
20 over said semiconductor chip and said resin layer.

25 2. A semiconductor device as claimed in
 claim 1, wherein said chamfer surface surrounds a top
 edge of said composite structure continuously, said
 top edge defining a top surface of said composite
 structure including a top surface of said resin layer.

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 3. A semiconductor device as claimed in
35 claim 1, wherein said chamfer surface is formed on a
 top edge of said semiconductor structure in
 correspondence to each of said plurality of corners,

1 said top edge defining a top surface of said composite
structure including a top surface of said resin layer.

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4. A semiconductor device as claimed in
claim 1, wherein said composite structure carries
another chamfer surface on a bottom edge of said
10 composite structure as a part of said side wall of
said composite structure, said bottom edge defining a
bottom surface of said composite structure.

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5. A semiconductor device as claimed in
claim 4, wherein said another chamfer surface extends
along said bottom edge continuously so as to surround
20 said composite structure laterally.

25 6. A semiconductor device as claimed in
claim 4, further comprising another resin layer on a
bottom principal surface of said semiconductor chip,
said another resin layer thereby forming a part of
said composite structure, said another chamfer surface
30 being formed on said semiconductor chip and said
another resin layer continuously.

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7. A semiconductor device as claimed in
claim 6, wherein said another chamfer surface is

1 formed along a bottom edge of said composite structure
continuously so as to surround said composite
structure laterally, said bottom edge defining a
bottom surface of said composite structure.

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8. A semiconductor device as claimed in
10 claim 1, wherein said semiconductor chip carries
another resin layer on a bottom principal surface
thereof.

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9. A semiconductor device as claimed in
claim 1, wherein said chamfer surface is provided on
each of said plurality of corners of said composite
20 structure such that said chamfer surface extends
substantially perpendicularly to said top principal
surface of said semiconductor chip.

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10. A semiconductor device as claimed in
claim 2, further including another chamfer surface
provided on each of said plurality of corners of said
30 composite structure such that said another chamfer
surface extends substantially perpendicularly to said
top principal surface of said semiconductor chip.

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11. A semiconductor device as claimed in

1 claim 5, further including an additional chamfer
surface on each of said plurality of corners of said
composite structure such that said additional chamfer
surface extends substantially perpendicularly to said
5 top surface of said semiconductor chip.

10 12. A semiconductor device as claimed in
claim 7, further including an additional chamfer
surface on each of said plurality of corners of said
composite structure such that said additional chamfer
surface extends substantially perpendicularly to said
15 top surface of said semiconductor chip.

20 13. A semiconductor device as claimed in
claim 2, wherein said resin layer has a surrounding
side wall inside said chamfer surface such that said
surrounding side wall is substantially perpendicularly
to said top principal surface of said semiconductor
25 chip.

30 14. A semiconductor device, comprising:
a semiconductor chip having a top principal
surface, said semiconductor chip carrying a plurality
of bump electrodes on said top principal surface;
a resin layer covering said top principal
35 surface of said semiconductor chip so as to seal said
semiconductor chip,
said semiconductor chip and said resin layer

1 thereby forming a composite semiconductor structure
defined by a side wall having a plurality of corners,
and

 a step surface formed in said resin layer
5 along said side wall of said composite structure.

10 15. A semiconductor device as claimed in
claim 14, wherein said step surface surrounds a top
edge of said composite structure continuously, said
top edge defining a top surface of said composite
structure including a top surface of said resin layer.

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 16. A semiconductor device as claimed in
20 claim 14, wherein said step surface is formed on a top
edge of said semiconductor structure in correspondence
to each of said plurality of corners, said top edge
defining a top surface of said composite structure
including a top surface of said resin layer.

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 17. A semiconductor device as claimed in
30 claim 14, wherein said composite structure carries
another resin layer on a bottom edge of said composite
structure as a part of said side wall of said
composite structure.

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1 18. A semiconductor device as claimed in
claim 17, further comprising another step surface in
said another resin layer along bottom edge of said
composite structure, said bottom edge defining a
5 bottom surface of said composite structure including a
bottom surface of said another resin layer.

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 19. A semiconductor device as claimed in
claim 18, wherein said another step surface is formed
in said another resin layer continuously so as to
surround said composite structure.

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 20. A semiconductor device as claimed in
20 claim 15, further comprising a chamfer surface
provided on each of said plurality of corners of said
composite structure such that said chamfer surface
extends substantially perpendicularly to said top
principal surface of said semiconductor chip.

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 21. A semiconductor device as claimed in
30 claim 19, further including a chamfer surface provided
on each of said plurality of corners of said composite
structure such that said chamfer surface extends
substantially perpendicularly to said top principal
surface of said semiconductor chip.

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1 22. A semiconductor device as claimed in
claim 20, further including another chamfer surface on
said bottom edge of said composite structure such that
said another chamfer surface surrounds said composite
5 structure laterally, said bottom edge defining a
bottom surface of said composite structure including a
bottom surface of said semiconductor chip.

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 23. A semiconductor device as claimed in
claim 15, further including a chamfer surface on said
bottom edge of said composite structure such that said
15 chamfer surface surrounds said composite structure
laterally, said bottom edge defining a bottom surface
of said composite structure including a bottom surface
of said semiconductor chip.

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 24. A semiconductor device, comprising:
a semiconductor chip having a top principal
25 surface, said semiconductor chip carrying a plurality
of bump electrodes on said top principal surface;
a resin layer covering said top principal
surface of said semiconductor chip so as to seal said
semiconductor chip,
30 a chamfer surface formed in a side wall of
said semiconductor chip as a part of said side wall
such that said chamfer surface surrounds said
semiconductor chip along a top edge thereof,
said resin layer covering said chamfer
35 surface.

1 25. A semiconductor device as claimed in
claim 24, further including: another chamfer surface
formed in said side wall of said semiconductor chip as
a part of said side wall such that said chamfer
5 surface surrounds said semiconductor chip along a
bottom edge thereof, said bottom edge defining a
bottom surface of said semiconductor chip, and another
resin layer provided on said bottom surface of said
semiconductor chip so as to cover said another chamfer
10 surface.

 26. A method of fabricating a semiconductor
15 device, comprising the steps of:
 forming a resin layer on a principal surface
of a semiconductor substrate;
 grooving said resin layer along a dicing
line on said semiconductor substrate to form a V-
20 shaped groove having a substantially V-shaped cross-
section such that said V-shaped groove reaches said
semiconductor substrate; and
 dicing, after said step of grooving, said
semiconductor substrate along said V-shaped groove by
25 forming a dicing groove with a width smaller than a
width of said V-shaped groove.

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 27. A method as claimed in claim 26,
wherein said step of grooving is conducted along said
dicing line for an entire length thereof on said
substrate.

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1 28. A method as claimed in claim 26,
 wherein said step of grooving is conducted in the
 vicinity of cross points of mutually crossing dicing
 lines to form said V-shaped groove in the form of
5 isolated cross-mark patterns.

10 29. A method as claimed in claim 35,
 wherein said step of grooving is conducted by a saw
 blade having a V-shaped saw blade edge between a pair
 of mutually parallel lateral surfaces, with such a
 depth that said V-shaped groove formed by said V-
15 shaped saw blade has a pair of lateral surfaces
 extending substantially perpendicularly to a principal
 surface of said semiconductor substrate in
 continuation to a V-shaped bottom of said V-shaped
 groove, and such that said lateral surfaces of said
20 saw blade engage said side walls of said V-shaped
 groove.

25 30. A method as claimed in claim 26,
 further comprising, after said step of forming said
 resin layer but before said step of grooving said
 resin layer, the step of reducing a thickness of said
30 semiconductor substrate by grinding a rear surface of
 said semiconductor substrate.

35 31. A method of fabricating a semiconductor
 device, comprising the steps of:

1 forming a resin layer on a principal surface
of a semiconductor substrate;
 dicing said semiconductor substrate along a
dicing line by forming a dicing groove through said
5 resin layer and through said semiconductor substrate;
and
 grooving, after said step of dicing of said
semiconductor substrate, said resin layer along said
dicing line to form a V-shaped groove having a
10 substantially V-shaped cross-section in said resin
layer such that said V-shaped groove has a width
larger than a width of said dicing groove and reaches
said semiconductor substrate.

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 32. A method as claimed in claim 31,
wherein said step of grooving is conducted along said
20 dicing line for an entire length thereof on said
substrate.

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 33. A method as claimed in claim 31,
wherein said step of grooving is conducted in the
vicinity of cross points of mutually crossing dicing
lines to form said V-shaped groove in the form of
30 isolated cross-mark patterns.

35 34. A method as claimed in claim 31,
wherein said semiconductor substrate is mounted on a
dicing apparatus by an adhesive tape.

1 35. A method as claimed in claim 31,
further comprising, after said step of forming said
resin layer but before said step of grooving, the step
of reducing a thickness of said substrate.

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 36. A method of fabricating a semiconductor
10 device, comprising the steps of:
 forming a resin layer on a principal surface
of a semiconductor substrate;
 grooving said resin layer along a dicing
line on said semiconductor substrate to form a first
15 groove having a substantially rectangular cross-
section and a first width in said resin layer; and
 dicing, after said step of grooving, said
semiconductor substrate along said first groove by
forming a second groove with a second width smaller
20 than said first width of said first groove.

25 37. A method as claimed in claim 36,
wherein said step of grooving is conducted along said
dicing line for an entire length thereof on said
substrate.

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 38. A method as claimed in claim 36,
wherein said step of grooving is conducted in the
35 vicinity of cross points of mutually crossing dicing
lines to form said first groove in the form of
isolated cross-mark patterns.

1 39. A method of fabricating a semiconductor device, comprising the step of:

adhering a semiconductor substrate on a dicing apparatus by an adhesive tape;

5 dicing said semiconductor substrate in a first direction such that said adhesive tape remains substantially intact;

dicing said semiconductor substrate in a second, different direction together with said adhesive tape, to form a plurality of adhesive strips each carrying thereon a plurality of semiconductor chips aligned in a row; and

10 applying a V-shaped saw blade having a V-shaped saw edge laterally to each of said adhesive strips such that said V-shaped saw blade cuts into a gap formed between a pair of adjacent semiconductor chips by said dicing step conducted in said first direction, said saw blade thereby forming a chamfer surface on a side wall of said semiconductor chips such that said chamfer surface extends, in each of said semiconductor chips, generally perpendicularly to a principal surface of said semiconductor chip.

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40. A method of fabricating a semiconductor device, comprising the steps of:

30 forming a V-shaped groove on a top surface of a semiconductor substrate, said semiconductor device carrying an electronic circuit on said top surface;

forming a resin layer on said top surface of said semiconductor substrate so as to fill said V-shaped groove; and

35 dicing said semiconductor substrate by a dicing saw having a blade width smaller than a width

1 of said V-shaped groove, along said V-shaped groove.

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41. A method as claimed in claim 40,
wherein said method further comprises the steps of:
forming another V-shaped groove on a bottom surface of
said semiconductor substrate; and forming another
10 resin layer on said bottom surface of said
semiconductor substrate so as to fill said another V-
shaped groove, and

wherein said dicing step is conducted by
said dicing saw such that said dicing saw cuts said
15 resin layer and said another resin layer
simultaneously.

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42. A method of fabricating a semiconductor
device, comprising the steps of:

slicing a semiconductor substrate from a
semiconductor ingot;

25 applying a resin layer on a first surface of
said semiconductor substrate such that said resin
layer has a planarized surface;

grinding a second surface of said
semiconductor substrate while using said planarized
30 surface of said resin layer as a reference surface, to
form a planarized surface on said second surface; and
grinding said first surface while using said
second, planarized surface as a reference surface, to
form a planarized surface on said first surface.

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1 43. A transportation device of a
semiconductor device, comprising:
a tray member adapted to support a
semiconductor device in a face-down state, said
5 semiconductor device carrying a plurality of bump
electrodes thereon, said tray member having an opening
for accommodating said bump electrodes when said
semiconductor device is mounted on said tray member;
and
10 a removable cap member provided on said tray
member removably, said removable cap member covering
said tray member in a state in which said
semiconductor device is mounted on said tray member,
wherein said tray member includes a chamfer
15 surface for engagement with a corresponding chamfer
surface formed on said semiconductor device.

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44. A transportation device as claimed in
claim 43, wherein said chamfer surface of said tray
member is formed so as to surround said opening
continuously.

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45. A transportation device as claimed in
30 claim 43, wherein said chamfer surface of said tray
member is formed on four corners of said opening.

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46. A transportation device of a
semiconductor device, comprising:

1 a tray member adapted to support a
semiconductor device in a face-down state, said
semiconductor device carrying a plurality of bump
electrodes thereon, said tray member having an opening
5 for accommodating said bump electrodes when said
semiconductor device is mounted on said tray member;
and

 a removable cap member provided on said tray
member removably, said removable cap member covering
10 said tray member in a state in which said
semiconductor device is mounted on said tray member,
 wherein said tray member includes a step
surface for engagement with a corresponding step
surface formed on said semiconductor device.

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 47. A transportation device as claimed in
20 claim 46, wherein said step surface of said tray
member is formed so as to surround said opening
continuously.

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 48. A transportation device as claimed in
claim 46, wherein said step surface of said tray
member is formed on four corners of said opening.

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 49. A method of fabricating a semiconductor
35 device, comprising the steps of:

 mounting a semiconductor device having a
chamfered surface and a plurality of bump electrodes

1 on a transportation device,

said transportation device comprising a tray member adapted to support said semiconductor device in a face-down state, said tray member having an opening
5 for accommodating said bump electrodes when said semiconductor device is mounted on said tray member, and a removable cap member provided on said tray member removably, said removable cap member covering said tray member in a state in which said
10 semiconductor device is mounted on said tray member, said tray member including a chamfer surface for engagement with said chamfer surface on said semiconductor device; and

transporting said semiconductor device in a
15 state mounted on said transportation device.

20 50. A method of fabricating a semiconductor device, comprising the steps of:

mounting a semiconductor device having a stepped surface and a plurality of bump electrodes on a transportation device,

25 said transportation device comprising a tray member adapted to support said semiconductor device in a face-down state, said tray member having an opening for accommodating said bump electrodes when said semiconductor device is mounted on said tray member,
30 and a removable cap member provided on said tray member removably, said removable cap member covering said tray member in a state in which said semiconductor device is mounted on said tray member, said tray member including a stepped surface for
35 engagement with said stepped surface on said semiconductor device; and

transporting said semiconductor device in a

1 state mounted on said transportation device.

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